

REMARKS

In the Office Action dated January 5, 2005, the Examiner rejected claims 16 and 17 under 35 U.S.C. §103(a). Claims 1-15, 18, and 19 were allowed.

Rejection under 35 U.S.C. § 103(a):

The Examiner rejects the claims based on Hall and Bortolini. Hall discloses a timing system where terminal devices measure timing offsets and sends them back to a base station to adjust a clock. However, as the Examiner points out, Hall does not disclose a vernier signal generator. For this the Examiner cites Bortolini. We have read through the Bortolini patent and nowhere in the patent does it describe anything close to a vernier signal.

The Bortolini patent describes clock synchronization within an optical switch. The switch has 256 optical connections that are divided into 8 subracks of 32 connections each. The entire system is controlled by a switch controller 101 that has a central timing unit 601 (he also calls it a "system timing unit" STU). Each subrack has its own clock 603 called a digital timing unit. Each subrack clock must synchronize to the central timing unit. There are ten signal paths between the system controller and each subrack and each path introduces its own jitter (this is what the Examiner refers to as "multiple timing paths set up through switching units"). The algorithm that he presents (Figure 7) simply determines which of the 10 paths are good (in case there is a failure in one of more path) and averages the timing offsets from the good paths to come up with a local

clock adjustment. Timing offset measurements are made by comparing the difference between two counters 617 and 612 (col. 10, lines 8-36).

Once all the subracks are synchronized to the central timing unit, the system controller picks one of the 256 optical inputs as a base to synchronize the central timing unit's clock. The Examiner points out that "local timing units synchronized to a centralized timing unit determine the difference in timing between external links and the local timing unit". This timing difference is measured by computing the difference of two counts (col. 12, lines 5-36). This timing information from each of the 256 optical inputs is passed up to the central timing unit, where the central timing unit picks the best one to use as a reference (from the Examiner's text: "information received by each of the external links designating the accuracy of the external link is transmitted to the central timing unit so that the central timing unit can select the external link having the highest accuracy").

The Examiner's argument that we can "apply Bortolini's synchronization of a timing unit to an external link into Hall's teaching of timing synchronization between a base oscillator and remote oscillator" does not apply to claims 16 and 17. The vernier signal generator of claim 16 is not described in either Hall or Bortolini. Bortolini describes a system that has many inputs, each with its own synchronization circuit, and a central timing unit that picks the best of the inputs to synchronize to based on it's "accuracy of frequency" (col. 13 lines 2-7). Claim 17 describes single receiver that chooses a portion of a vernier signal is the best match to the oscillator. The


synchronization choice of Bortolini's system is done for different reasons and by different methods than the synchronization choice done in claim 17. Thus, claims 16 and 17 are neither disclosed, taught, nor suggested by the prior art of record. Applicant respectfully requests that the rejection be withdrawn and the application passed to issue.

Conclusion

In view of the above Remarks, Applicant submits that the present application is in condition for allowance, and seeks early indication of the same. If the Examiner requires further information with respect to this application, the Examiner is invited to contact Applicant's attorney at (847) 537-3537 for a telephonic interview.

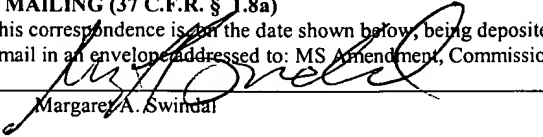
Respectfully submitted,

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